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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of
Toshiharu Furukawa et al

Examiner: Loke, Steven Ho Yin

Serial No: 09/944,665

Art Unit: 2811

Filed: August 31, 2001

Docket: BUR919990305US1

For: Vertical Dual Gate Field Effect
Transistor

Dated: April 5, 2004

Assistant Commissioner for Patents
United States Patent and Trademark Office
Washington, D.C. 20231AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In reply to the Office Action dated Dec. 3, 2003, Applicants respectfully request reconsideration of the outstanding objections and rejections, and reexamination of the present application in light of the following amendments and remarks.

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that this paper is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Dated: April 5, 2004


Arnette Dodge

Serial No. 09/944,665

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claim 35 "SOT" has been replaced with "silicon-on-insulator".

Claim 3 has been amended for consistency in the application.

Also, the rejections based on §112 have been addressed, by amending "an insulating sidewall", "said trench", "first diffusion" and "second diffusion", as required by the Examiner.

In view of the foregoing amendments and remarks, Applicants submit that all of the claims in the present application are in condition for allowance. Accordingly, it is respectfully requested that the Examiner pass the present application to issue.

If any fees, including extension of time fees, are due as a result of this response, please charge IBM Corp. Deposit Account No. 09-0456. This authorization is intended to act as a constructive petition for an extension of time, should an extension of time be needed as a result of this response. The Examiner is invited to telephone the undersigned if this would in any way advance the prosecution of this application.

Respectfully submitted,

FOR: Toshiharu Furukawa, et al

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Date: APR. 5, 2004

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